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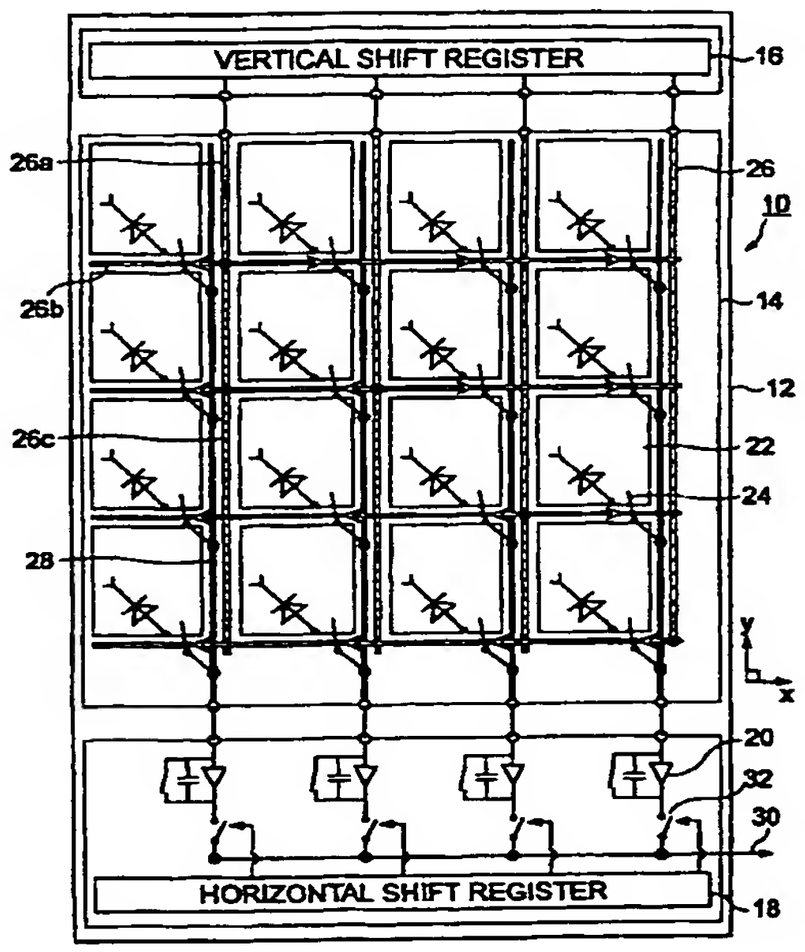
(54) SOLID-STATE IMAGING DEVICE AND SOLID-STATE IMAGING ARRAY

(57) A solid-state image sensing device 10 mainly includes a light-receiving portion 14 formed on a substrate 12, a vertical shift register 16 formed to face one side of the light-receiving portion 14, and a horizontal shift register 18 and charge amplifiers 20 formed to face the opposite side of the light-receiving portion 14. The light-receiving portion 14 is formed from M x N photodiodes 22, and each photodiode 22 has a gate switch 24. The control terminals of the gate switches 24 are connected to the vertical shift register 16 via gate lines 26 in units of rows. The gate lines 26 have compensation lines 26c so as to make almost equal the capacitances of the gate lines 26 connected in units of rows. Accordingly, a plurality of solid-state image sensing devices 10 can be easily arrayed without any dead zone and can increase the light-receiving area.

Fig.1



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can be arrayed without any dead zone, on a side facing the side on which the vertical and horizontal shift registers are formed.

[0010] These solid-state image sensing devices can be formed into a solid-state image sensing device array in which the devices are arrayed on the above-mentioned sides without any dead zone.

[0011] Further, the second wiring lines have the compensation portions for making the capacitances of the second wiring lines almost equal in units of rows. The compensation portions can compensate for the difference between capacitances caused by the difference between the lengths of the second wiring lines in units of rows, and can make the capacitances of the second wiring lines in units of rows almost equal.

Brief Description of the Drawings

[0012]

Fig. 1 is a diagram showing the arrangement of a solid-state image sensing device according to the first embodiment;
Fig. 2 is a diagram showing the arrangement of a solid-state image sensing device according to the second embodiment;
Fig. 3 is a diagram showing the arrangement of a solid-state image sensing device according to the third embodiment;
Fig. 4 is a diagram showing the arrangement of a solid-state image sensing device according to the fourth embodiment;
Fig. 5 is a view showing an example of a solid-state image sensing device array formed using the solid-state image sensing device shown in Fig. 1;
Fig. 6 is a view showing an example of a solid-state image sensing device array formed using the solid-state image sensing device shown in Fig. 4; and
Fig. 7 is a view showing another example of the solid-state image sensing device array formed using the solid-state image sensing device shown in Fig. 4.

Best Mode of Carrying Out the Invention

[0013] A solid-state image sensing device according to the first embodiment of the present invention will be described with reference to Fig. 1. First, the arrangement of the solid-state image sensing device according to this embodiment will be explained. Fig. 1 is a diagram showing the arrangement of the solid-state image sensing device according to the first embodiment. For descriptive convenience, the right-to-left direction in Fig. 1 will be referred to as an x-axis direction (positive toward right); and the top-to-bottom direction, as a y-axis direction (positive toward top).

[0014] In a solid-state image sensing device 10 according to the first embodiment, as shown in Fig. 1, a light-receiving portion 14, vertical shift register 16, horizontal shift register 18, and charge amplifiers (amplifier portions) 20 are formed on a substrate 12. They will be described in detail.

[0015] The light-receiving portion 14 is constituted by arraying on the substrate 12 a plurality of photodiodes (photoelectric converters) 22 for accumulating a charge amount corresponding to the light incident intensity. More specifically, the light-receiving portion 14 is made up of M x N photodiodes 22 arrayed in M rows in the y-axis direction and N columns in the x-axis direction (M and N are natural numbers).

[0016] Each photodiode 22 constituting the light-receiving portion 14 has a gate switch (switch forming the first switch group) 24 having one terminal connected to the photodiode 22 and the other terminal connected to a signal readout line (to be described later). When the gate switch 24 is open, charges by optical absorption are accumulated in the photodiode 22. If the gate switch 24 is closed, charges accumulated in the photodiode 22 are read out to the signal readout line (to be described later).

[0017] The vertical shift register 16 is formed on the substrate 12 on the upper side of the light-receiving portion 14 in the y-axis direction. The vertical shift register 16 outputs a vertical scanning signal for opening/closing the gate switch 24.

[0018] The control terminal of each gate switch 24 and the vertical shift register 16 are connected by a corresponding gate line (second wiring line) 26. This allows opening/closing the gate switch 24 by a vertical scanning signal output from the vertical shift register 16. The gate lines 26 include, specifically, N vertical lines 26a which extend from the vertical shift register 16 in the y-axis direction between the columns of the photodiodes 22 arrayed on the light-receiving portion 14, and N horizontal lines 26b which are respectively connected to the vertical lines 26a, and extend in the x-axis direction between the rows of the photodiodes 22 arrayed on the light-receiving portion 14. Each horizontal line 26b is connected to the control terminals of gate switches 24 existing on the same row. Therefore, the vertical shift register 16 and the control terminals of the gate switches 24 are connected in units of rows. Further, the vertical lines 26a of the gate lines 26 have compensation lines (compensation wiring lines) 26c so as to make almost equal the capacitances of the gate lines 26 connected in units of rows, more specifically, make the lengths of the vertical lines 26a of the gate lines 26 equal. That is, the lengths of the horizontal lines 26b are equal to each other, whereas the lengths of the vertical lines 26a including the compensation lines 26c are also equal to each other.

[0019] M signal readout lines (first wiring lines) 28 each connected to the other terminals of the gate switches 24 in units of columns are formed between the columns of the photodiodes 22 arrayed on the light-receiving portion 14. The M signal readout lines 28 are

state image sensing device 40 according to the second embodiment is different from the solid-state image sensing device 10 according to the first embodiment in the following point. That is, in the solid-state image sensing device 10 according to the first embodiment, the compensation lines 26c for making the lengths of the vertical lines 26a of the gate lines 26 equal are formed to make almost equal the capacitances of the gate lines 26 connected in units of rows. To the contrary, in the solid-state image sensing device 40 according to the second embodiment, capacitors 42 are connected to respective vertical lines 26a of gate lines 26 so as to make almost equal the capacitances of the gate lines 26 connected in units of rows. As the length of the vertical line 26a of each gate line 26 becomes shorter, the capacitance of the capacitor 42 connected to the vertical line 26a becomes larger.

[0029] A light-shielding line 44 of polysilicon or aluminum having almost the same width as that of the vertical line 26a is formed at a portion where no vertical line 26a is formed in the extending direction of the vertical line 26a between the columns of photodiodes 22 arrayed on a light-receiving portion 14. Since the light-shielding line 44 having almost the same width as that of the vertical line 26a is formed at a portion where no vertical line 26a is formed, the opening areas of the photodiodes 22 can be made equal even if both a portion where the vertical line 26a is formed and a portion where no vertical line 26a is formed exist between the columns of the photodiodes 22 arrayed on the light-receiving portion 14. Thus, generation of a nonuniform image by the difference in opening area can also be prevented.

[0030] In the solid-state image sensing device 40 according to this embodiment, as in the solid-state image sensing device 10 according to the first embodiment, the light-receiving area can be easily increased without any dead zone.

[0031] The solid-state image sensing device 40 according to this embodiment uses the capacitors 42 to make almost equal the capacitances of the gate lines 26 connected in units of rows. Therefore, the capacitances of the gate lines 26 connected in units of rows can be easily made almost equal, compared to a case in which the compensation lines 26c are formed. The resistances of the gate lines 26 cannot be strictly made equal, compared to a case in which the compensation lines 26c are formed. However, mainly the difference between the capacitances of the gate lines affects the transmission characteristic of the vertical scanning signal to generate a nonuniform image. Considering this, generation of a nonuniform image can be easily and effectively prevented using the capacitors 42.

[0032] A solid-state image sensing device according to the third embodiment of the present invention will be described with reference to Fig. 3. Fig. 3 is a diagram showing the arrangement of the solid-state image sensing device according to this embodiment. A solid-state image sensing device 50 according to the third embodiment is different from the solid-state image sensing device 10 according to the first embodiment in the following point. That is, in the solid-state image sensing device 10 according to the first embodiment, the compensation lines 26c for making the lengths of the vertical lines 26a of the gate lines 26 equal are formed to make almost equal the capacitances of the gate lines 26 connected in units of rows. To the contrary, in the solid-state image sensing device 50 according to the third embodiment, conductive pads 52 are formed on vertical lines 26a of gate lines 26 so as to make almost equal the capacitances of the gate lines 26 connected in units of rows. AS the length of the vertical line 26a of each gate line 26 becomes shorter, the area of the conductive pad 52 formed on the vertical line 26a becomes larger. The conductive pad 52 functions as a capacitor in cooperation with a substrate 12 and another conductive portion. For a larger area, the capacitance increases.

[0033] Further, similar to the solid-state image sensing device 40 according to the second embodiment, a light-shielding line 44 is formed at a portion where no vertical line 26a is formed in the extending direction of the vertical line 26a between the columns of photodiodes 22 arrayed on a light-receiving portion 14. The light-shielding line 44 prevents generation of a nonuniform image owing to the difference in opening area.

[0034] In the solid-state image sensing device 50 according to this embodiment, as in the solid-state image sensing device 10 according to the first embodiment, the light-receiving area can be easily increased without any dead zone.

[0035] In the solid-state image sensing device 50 according to this embodiment, as in the solid-state image sensing device 40 according to the second embodiment, the resistances of the gate lines 26 cannot be strictly made equal. However, mainly the difference between the capacitances of the gate lines affects the transmission characteristic of the vertical scanning signal to generate a nonuniform image. Considering this, generation of a nonuniform image can be easily and effectively prevented using the conductive pads 52.

[0036] A solid-state image sensing device according to the fourth embodiment of the present invention will be described with reference to Fig. 4. Fig. 4 is a diagram showing the arrangement of the solid-state image sensing device according to this embodiment. A solid-state image sensing device 60 according to the fourth embodiment is different from the solid-state image sensing device 10 according to the first embodiment in the following point. That is, in the solid-state image sensing device 10 according to the first embodiment, the vertical and horizontal shift registers 16 and 18 are respectively formed on two facing sides of the light-receiving portion 14. To the contrary, in the solid-state image sensing device 60 according to the fourth embodiment, both vertical and horizontal shift registers 16 and 18 are formed on a predetermined side (lower

formed from the solid-state image sensing devices 60_1 to 60_3; a second array 702, from the solid-state image sensing devices 60_4 to 60_6; and a third array 703, from the solid-state image sensing devices 60_7 to 60_9.

[0049] The shift register portion 19 of the first array 701 is set as an upper side in Fig. 7, and the shift register portion 19 of the second array 702 is set as a lower side. The lower sides of the solid-state image sensing devices 60_2 and 60_3 opposite to the shift register portion 19 are arranged in contact with the upper sides of the solid-state image sensing devices 60_4 and 60_5 opposite to the shift register portion 19. In addition, the shift register portion 19 of the third array 703 is set as a left side in Fig. 7. The upper and right sides of the upper solid-state image sensing device 60_7 perpendicular to and opposite to the shift register portion 19 are arranged in contact with the lower side of the solid-state image sensing device 60_1 and the left side of the solid-state image sensing device 60_4, respectively. This can also realize the solid-state image sensing device array 700 free from any dead zone between the solid-state image sensing devices 60_1 to 60_9.

Industrial Applicability

[0050] The present invention can be applied as a solid-state image sensing device capable of attaining a large light-receiving area without any dead zone as an insensible region. Since the vertical and horizontal shift registers are arranged on two facing sides or a predetermined side of a light-receiving portion, the solid-state image sensing device can be easily manufactured and arrayed. Consequently, the light-receiving area can be easily increased, and any number of solid-state image sensing devices can be arrayed without any dead zone.

[0051] In the solid-state image sensing device of the present invention, the second wiring lines have the compensation portions for making the capacitances of the second wiring lines almost equal in units of rows. The compensation portions can compensate for the difference between capacitances by the difference between the lengths of the second wiring lines in units of rows. As a result, generation of a nonuniform image by the capacitance difference can be prevented.

Claims

1. A solid-state image sensing device characterized by comprising:

   a light-receiving portion having a plurality of photoelectric converters arrayed in M rows and N columns on a substrate;
   first wiring lines formed in units of columns;
   a first switch group including a plurality of switches for connecting the photoelectric converters to said first wiring lines in units of columns;
   a vertical shift register for outputting a vertical scanning signal for opening/closing the switches forming said first switch group in units of rows;
   second wiring lines for connecting control terminals of the switches forming said first switch group to said vertical shift register in units of rows;
   a second switch group including a plurality of switches for connecting said first wiring lines to a signal output line; and
   a horizontal shift register for outputting a horizontal scanning signal for opening/closing the switches forming said second switch group in units of columns,
   wherein said vertical and horizontal shift registers are respectively arranged on two facing sides of said light-receiving portion, and
   said second wiring lines have compensation portions for making capacitances of said second wiring lines almost equal in units of rows.

2. A solid-state image sensing device characterized by comprising:

   a light-receiving portion having a plurality of photoelectric converters arrayed in M rows and N columns on a substrate;
   first wiring lines formed in units of columns;
   a first switch group including a plurality of switches for connecting the photoelectric converters to said first wiring lines in units of columns;
   a vertical shift register for outputting a vertical scanning signal for opening/closing the switches forming said first switch group in units of rows;
   second wiring lines for connecting control terminals of the switches forming said first switch group to said vertical shift register in units of rows;
   a second switch group including a plurality of switches for connecting said first wiring lines to a signal output line; and
   a horizontal shift register for outputting a horizontal scanning signal for opening/closing the switches forming said second switch group in units of columns,
   wherein said vertical and horizontal shift registers are arranged on a predetermined side of said light-receiving portion, and
   said second wiring lines have compensation portions for making capacitances of said second wiring lines almost equal in units of rows.

3. A solid-state image sensing device according to claim 1 or 2, characterized by further comprising, on a side on which said horizontal shift register is

Fig.1

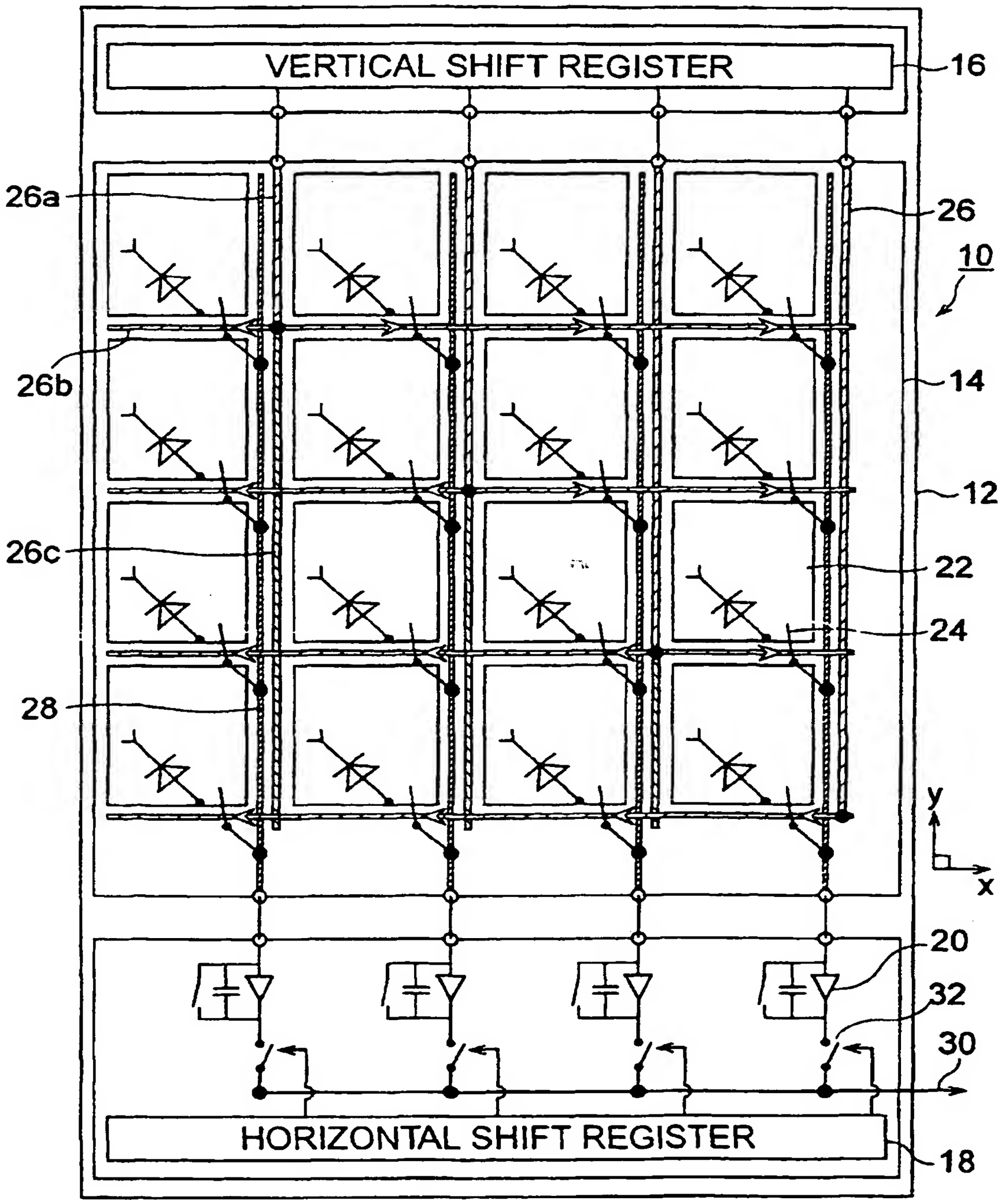


Fig.3

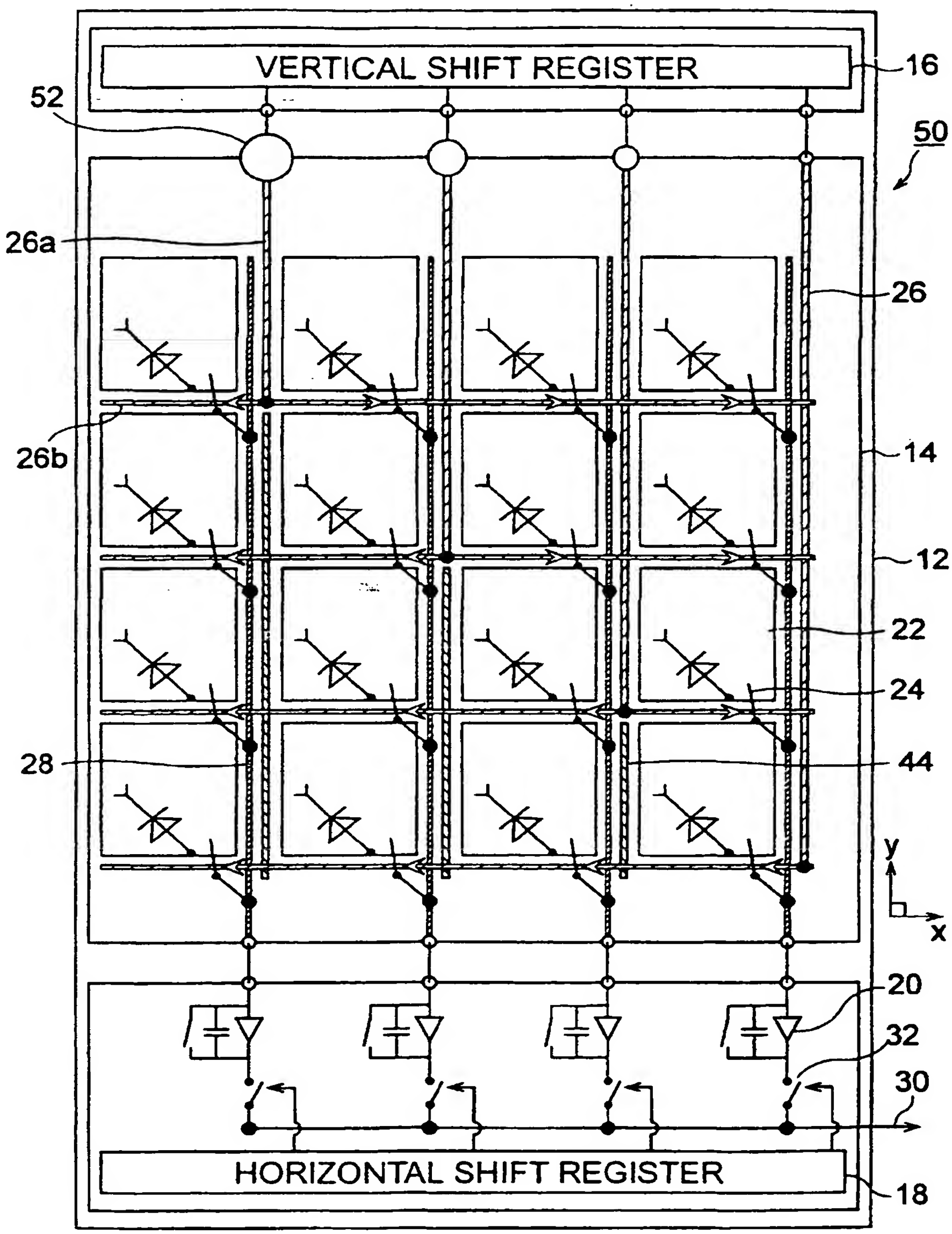


Fig.5

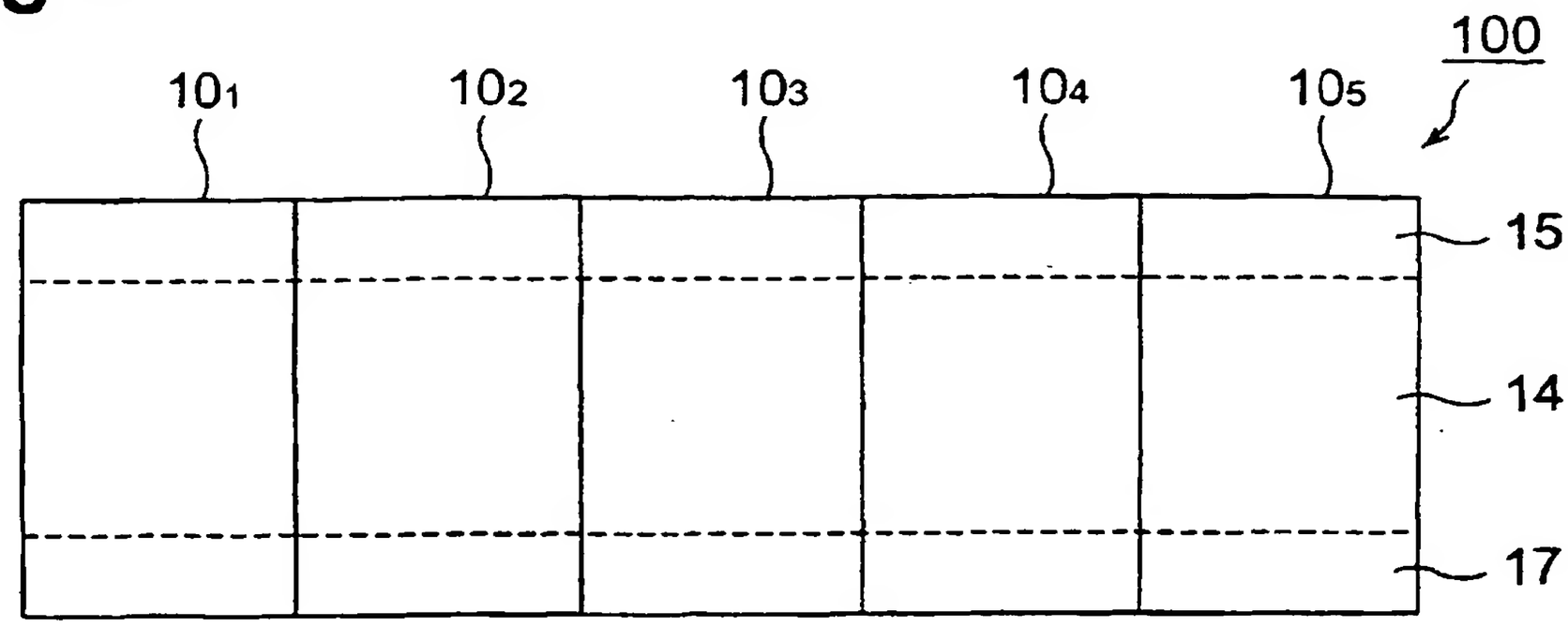
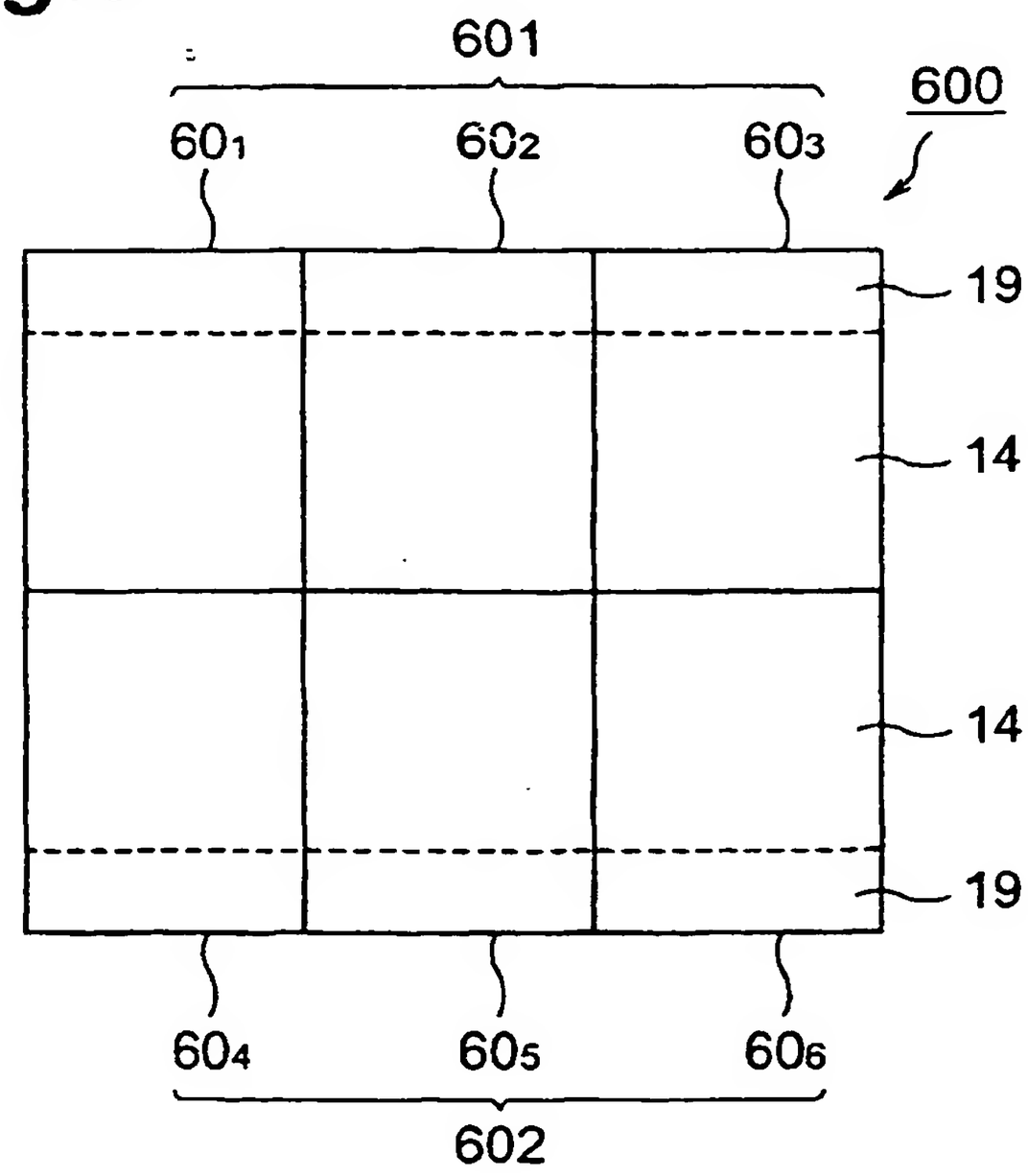


Fig.6



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP99/03856

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[6] H01L27/146, H04N5/335

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[6] H01L27/146, H04N5/335

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-1999
Kokai Jitsuyo Shinan Koho 1971-1999 Jitsuyo Shinan Toroku Koho 1996-1999

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 6-260630, A (Nikon Corp.), 16 September, 1994 (16. 09. 94), Full text ; Figs. 1 to 5 (Family: none)	1-8
A	JP, 61-253859, A (Hitachi,Ltd.), 11 November, 1986 (11. 11. 86), Claims ; page 3, upper left column, line 17 to lower left column, line 9 ; Figs. 1, 2 (Family: none)	1-8
A	JP, 63-257267, A (Seiko Instruments Inc.), 25 October, 1988 (25. 10. 88), Claims ; Examples ; Fig. 1 (Family: none)	1-8
A	JP, 8-181821, A (Canon Inc.), 12 July, 1996 (12. 07. 96), Full text ; Figs. 1 to 9 (Family: none)	1-8

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
12 October, 1999 (12. 10. 99)	19 October, 1999 (19. 10. 99)
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